



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark Moyer & Jeffrey Byrne  
Assignee: Lattice Semiconductor Corporation  
Title: Continuous Self-Verify Of Configuration Memory In Programmable  
Logic Devices  
Serial No.: 10/676,494 Filing Date: 09/30/2003  
Examiner: Unassigned Group Art Unit: 2124  
Docket No.: M-15194 US

Irvine, California  
February 3, 2004

Attn: Official Draftsperson  
COMMISSIONER FOR PATENTS  
Alexandria, VA 22313-1450

**SUBMISSION OF FORMAL DRAWINGS**

Dear Sir:

Applicants submit three (3) sheets of formal drawings, consisting of Figures 1, 2, and 3, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (949) 752-7040.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on February 3, 2004.

Eric Hoover

2/3/04

Date of Signature

Respectfully submitted,

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